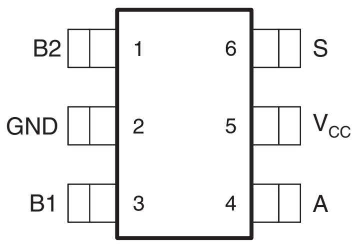
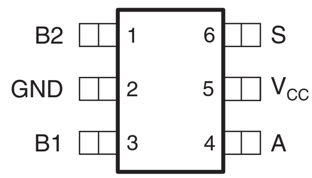
FEATURES

- 1.65-V to 5.5-V V_{CC} Operation
- Useful for Both Analog and Digital Applications
- Specified Break-Before-Make Switching
- Rail-to-Rail Signal Handling
- High Degree of Linearity
- High Speed, Typically 0.5 ns (V_{CC} = 3 V, C_L = 50 pF)
- Low On-State Resistance, Typically ≈6 Ω (V_{CC} = 4.5 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

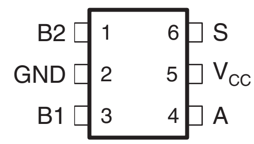
DBV PACKAGE
(TOP VIEW)



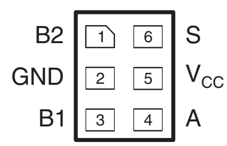
DCK PACKAGE
(TOP VIEW)



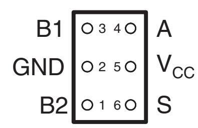
DRL PACKAGE
(TOP VIEW)



DRY PACKAGE
(TOP VIEW)



YZP PACKAGE
(BOTTOM VIEW)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single-pole, double-throw (SPDT) analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G3157 can handle both analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

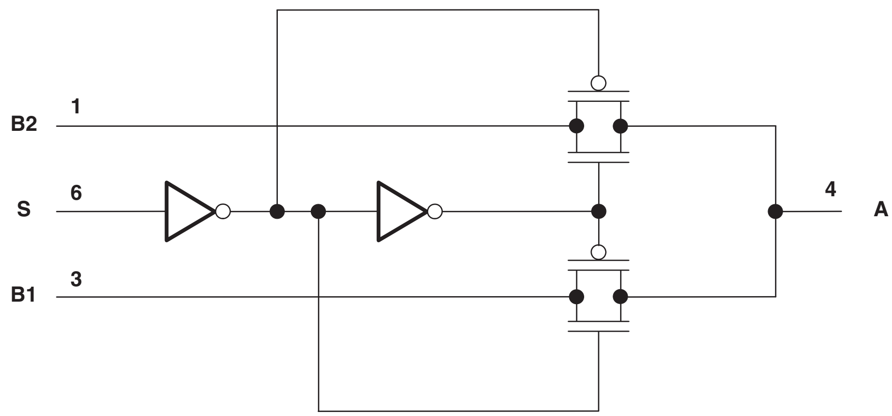
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC1G3157YZPR	_ _ _ C5_
	SON – DRY	Reel of 5000	SN74LVC1G3157DRYR	C5_
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G3157DBVR	CC5_
	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1G3157DCKR	C5_
	SOT (SOT-553) – DRL	Reel of 4000	SN74LVC1G3157DRLR	C5_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DBV/DCK/DRL/DRY: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

CONTROL INPUT S	ON CHANNEL
L	B1
H	B2

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.5	6.5	V
V_{IN}	Control input voltage range(2)(3)		–0.5	6.5	V
$V_{I/O}$	Switch I/O voltage range(2)(3)(4)(5)		–0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
I_{IOK}	I/O port diode current	$V_{I/O}$ < 0 or $V_{I/O}$ > V_{CC}		±50	mA
$I_{I/O}$	On-state switch current(6)	$V_{I/O}$ = 0 to V_{CC}		±128	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(7)	DBV package		165	°C/W
		DCK package		259	
		DRL package		142	
		DRY package		234	
		YZP package		123	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.
(5) V_I, V_O, V_A, and V_{Bn} are used to denote specific conditions for $V_{I/O}$.
(6) I_I, I_O, I_A, and I_{Bn} are used to denote specific conditions for $I_{I/O}$.
(7) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}			1.65	5.5	V
$V_{I/O}$			0	V_{CC}	V
V_{IN}			0	5.5	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V	$V_{CC} \times 0.75$		V
		V_{CC} = 2.3 V to 5.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V		$V_{CC} \times 0.25$	V
		V_{CC} = 2.3 V to 5.5 V		$V_{CC} \times 0.3$	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.65 V to 1.95 V		20	ns/V
		V_{CC} = 2.3 V to 2.7 V		20	
		V_{CC} = 3 V to 3.6 V		10	
		V_{CC} = 4.5 V to 5.5 V		10	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			V_{CC}	MIN	TYP[1]	MAX	UNIT
r_{on}	On-state switch resistance[2]	See Figure 1 and Figure 2	V_I = 0 V	I_O = 4 mA	1.65 V		11	20	Ω
			V_I = 1.65 V	I_O = –4 mA			15	50	
			V_I = 0 V	I_O = 8 mA	2.3 V		8	12	
			V_I = 2.3 V	I_O = –8 mA			11	30	
			V_I = 0 V	I_O = 24 mA	3 V		7	9	
			V_I = 3 V	I_O = –24 mA			9	20	
			V_I = 0 V	I_O = 30 mA	4.5 V		6	7	
			V_I = 2.4 V	I_O = –30 mA			7	12	
			V_I = 4.5 V	I_O = –30 mA			7	15	
r_{range}	On-state switch resistance over signal range[2][3]	$0 \le V_{Bn} \le V_{CC}$ (see Figure 1 and Figure 2)		I_A = –4 mA	1.65 V			140	Ω
				I_A = –8 mA	2.3 V			45	
				I_A = –24 mA	3 V			18	
				I_A = –30 mA	4.5 V			10	
Δr_{on}	Difference of on-state resistance between switches[2][4][5]	See Figure 1	V_{Bn} = 1.15 V	I_A = –4 mA	1.65 V		0.5		Ω
			V_{Bn} = 1.6 V	I_A = –8 mA	2.3 V		0.1		
			V_{Bn} = 2.1 V	I_A = –24 mA	3 V		0.1		
			V_{Bn} = 3.15 V	I_A = –30 mA	4.5 V		0.1		
$r_{on(flat)}$	ON resistance flatness[2][4][6]	$0 \le V_{Bn} \le V_{CC}$		I_A = –4 mA	1.65 V		110		Ω
				I_A = –8 mA	2.3 V		26		
				I_A = –24 mA	3 V		9		
				I_A = –30 mA	4.5 V		4		

(1) T_A = 25°C
(2) Measured by the voltage drop between I/O pins at the indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A or B) ports.
(3) Specified by design
(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$ measured at identical V_{CC}, temperature, and voltage levels
(5) This parameter is characterized, but not tested in production.
(6) Flatness is defined as the difference between the maximum and minimum values of ON resistance over the specified range of conditions.

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
I_{off}[7]	Off-state switch leakage current		$0 \le V_I, V_O \le V_{CC}$ (see Figure 3)	1.65 V to 5.5 V			±1	µA
						±0.05	±1[1]	
$I_{S(on)}$	On-state switch leakage current		$V_I = V_{CC}$ or GND, V_O = Open (see Figure 4)	5.5 V			±1	µA
							±0.1[1]	
I_{IN}	Control input current		$0 \le V_{IN} \le V_{CC}$	0 V to 5.5 V			±1	µA
						±0.05	±1[1]	
I_{CC}	Supply current		$V_{IN} = V_{CC}$ or GND	5.5 V		1	10	µA
ΔI_{CC}	Supply-current change		$V_{IN} = V_{CC} - 0.6$ V	5.5 V			500	µA
C_{in}	Control input capacitance	S		5 V		2.7		pF
$C_{io(off)}$	Switch input/ouput capacitance	Bn		5 V		5.2		pF
$C_{io(on)}$	Switch input/ouput capacitance	Bn		5 V		17.3		pF
		A				17.3		

(7) I_{off} is the same as $I_{S(off)}$ (off-state switch leakage current).

Analog Switch Characteristics

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response[1] (switch on)	A or Bn	Bn or A	R_L = 50 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	300	MHz
				2.3 V	300	
				3 V	300	
				4.5 V	300	
Crosstalk[2] (between switches)	B1 or B2	B2 or B1	R_L = 50 Ω, f_{in} = 10 MHz (sine wave) (see Figure 7)	1.65 V	–54	dB
				2.3 V	–54	
				3 V	–54	
				4.5 V	–54	
Feed-through attenuation[2] (switch off)	A or Bn	Bn or A	C_L = 5 pF, R_L = 50 Ω, f_{in} = 10 MHz (sine wave) (see Figure 8)	1.65 V	–57	dB
				2.3 V	–57	
				3 V	–57	
				4.5 V	–57	
Charge injection[3]	S	A	C_L = 0.1 nF, R_L = 1 MΩ (see Figure 9)	3.3 V	3	pC
				5 V	7	
Total harmonic distortion	A or Bn	Bn or A	V_I = 0.5 Vp-p, R_L = 600 Ω, f_{in} = 600 Hz to 20 kHz (sine wave) (see Figure 10)	1.65 V	0.1	%
				2.3 V	0.025	
				3 V	0.015	
				4.5 V	0.01	

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads –3 dB.
(2) Adjust f_{in} voltage to obtain 0 dBm at input.
(3) Specified by design

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5 and Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}[1]	A or Bn	Bn or A		2		1.2		0.8		0.3	ns
t_{en}[2]	S	Bn	7	24	3.5	14	2.5	7.6	1.7	5.7	ns
t_{dis}[3]			3	13	2	7.5	1.5	5.3	0.8	3.8	
$t_{B\text{-}M}$[4]			0.5		0.5		0.5		0.5		ns

(1) t_{pd} is the slower of t_{PLH} or t_{PHL}. The propagation delay is calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(2) t_{en} is the slower of t_{PZL} or t_{PZH}.
(3) t_{di}s is the slower of t_{PLZ} or t_{PHZ}.
(4) Specified by design

PARAMETER MEASUREMENT INFORMATION

SW	S
1	V_{IL}
2	V_{IH}

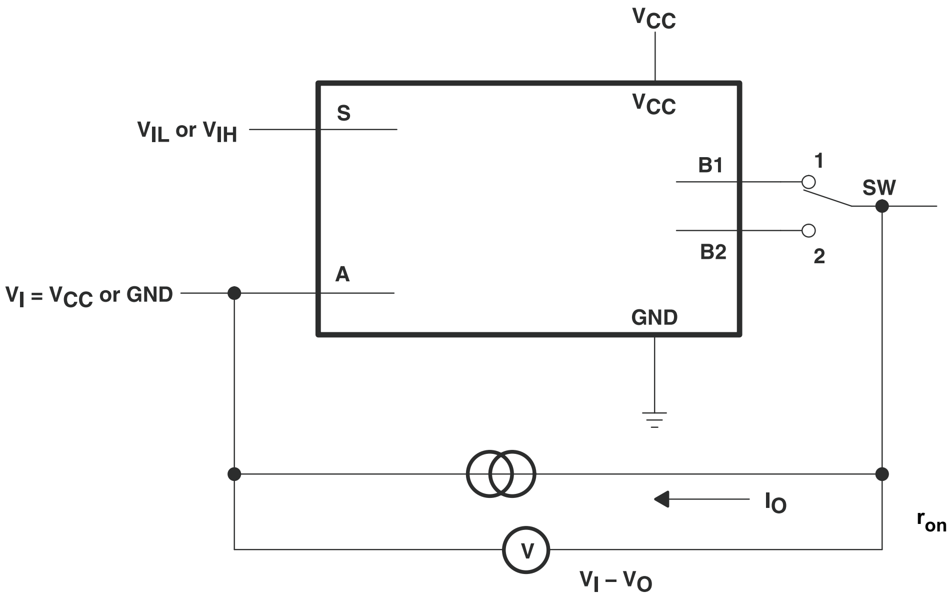


Figure 1. On-State Resistance Test Circuit

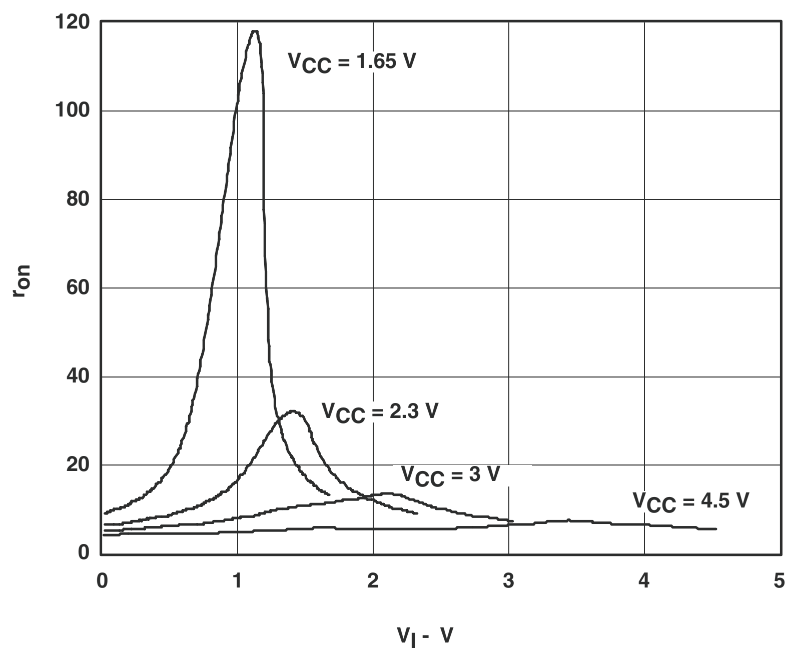
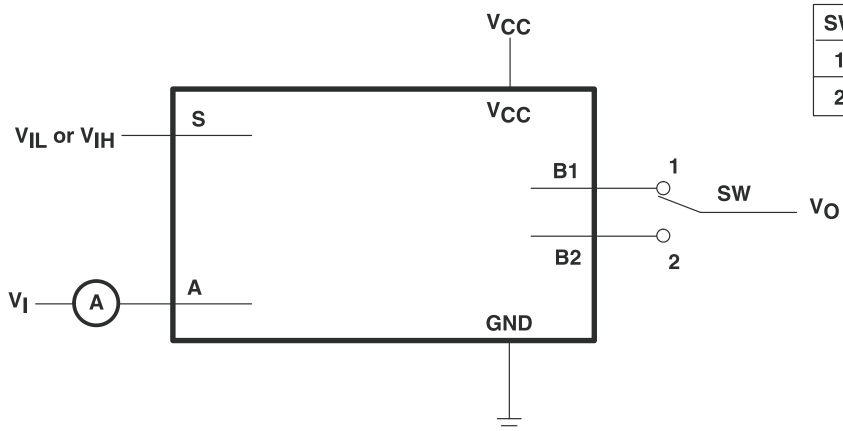


Figure 2. Typical r_{on} as a Function of Input Voltage (V_I) for V_I = 0 to V_{CC}

PARAMETER MEASUREMENT INFORMATION (continued)

SW	S
1	V_{IL}
2	V_{IH}



Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

Figure 3. Off-State Switch Leakage-Current Test Circuit

SW	S
1	V_{IL}
2	V_{IH}

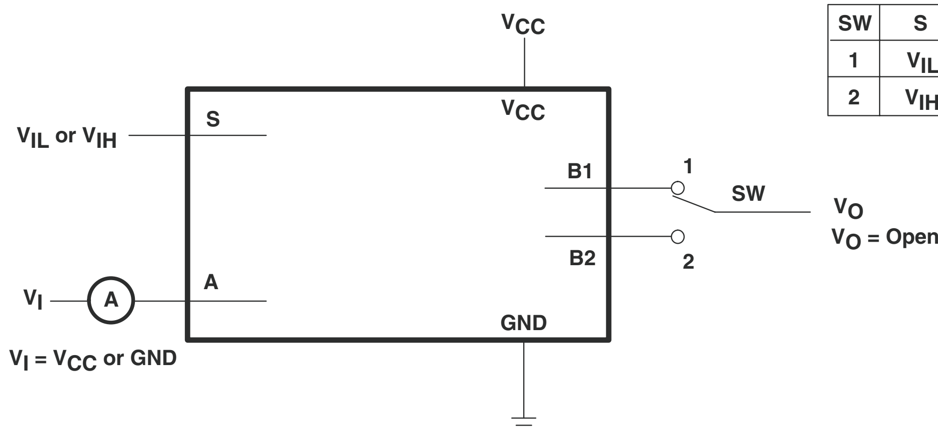
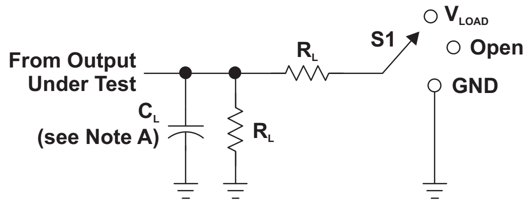


Figure 4. On-State Switch Leakage-Current Test Circuit

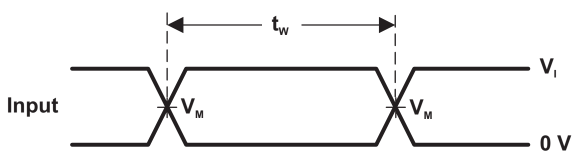
PARAMETER MEASUREMENT INFORMATION (continued)



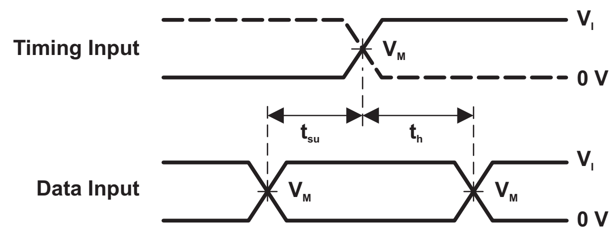
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

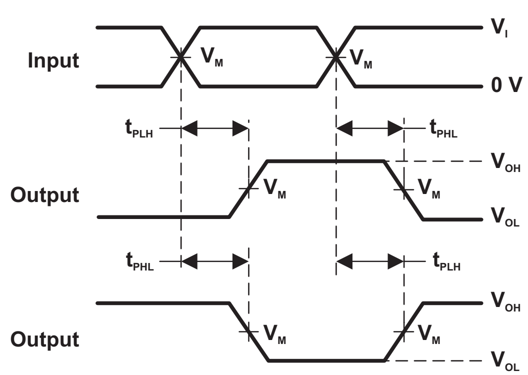
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



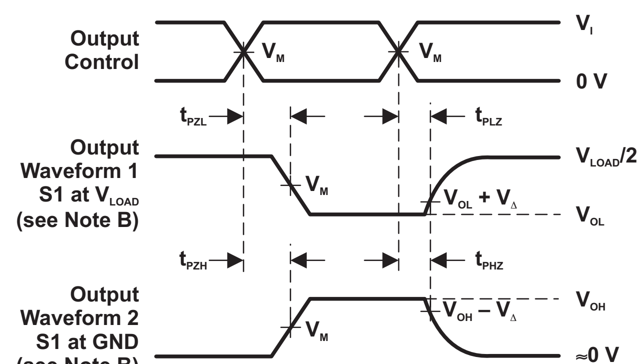
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

SW	S
1	V_{IL}
2	V_{IH}

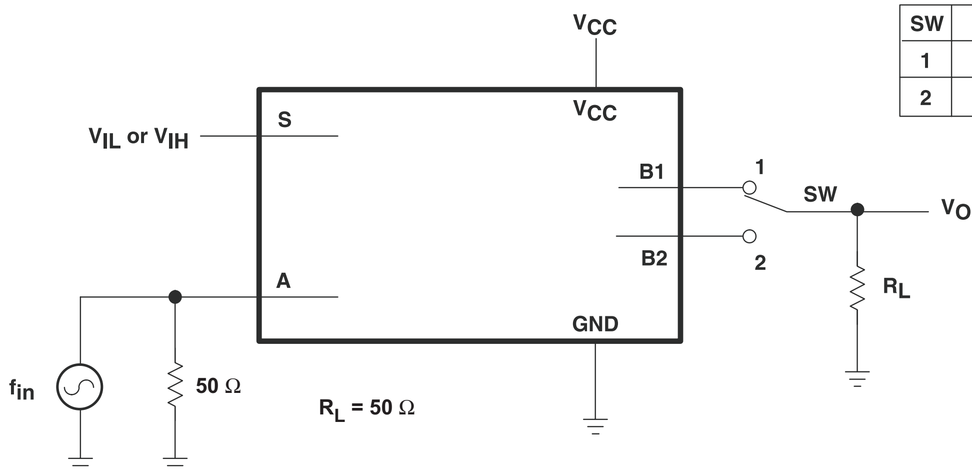


Figure 6. Frequency Response (Switch On)

S	TEST CONDITION
V_{IL}	$20\log_{10}(V_{O2}/V_I)$
V_{IH}	$20\log_{10}(V_{O1}/V_I)$

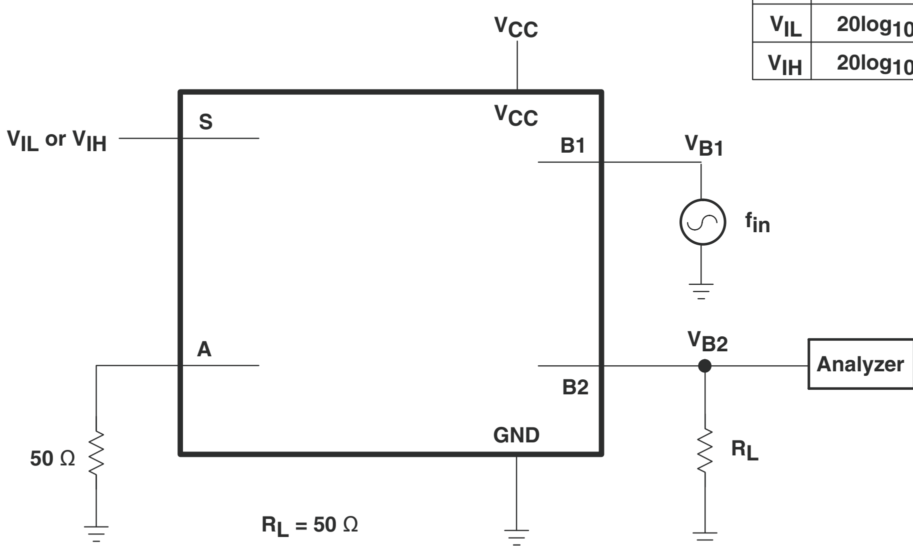


Figure 7. Crosstalk (Between Switches)

PARAMETER MEASUREMENT INFORMATION (continued)

SW	S
1	V_{IL}
2	V_{IH}

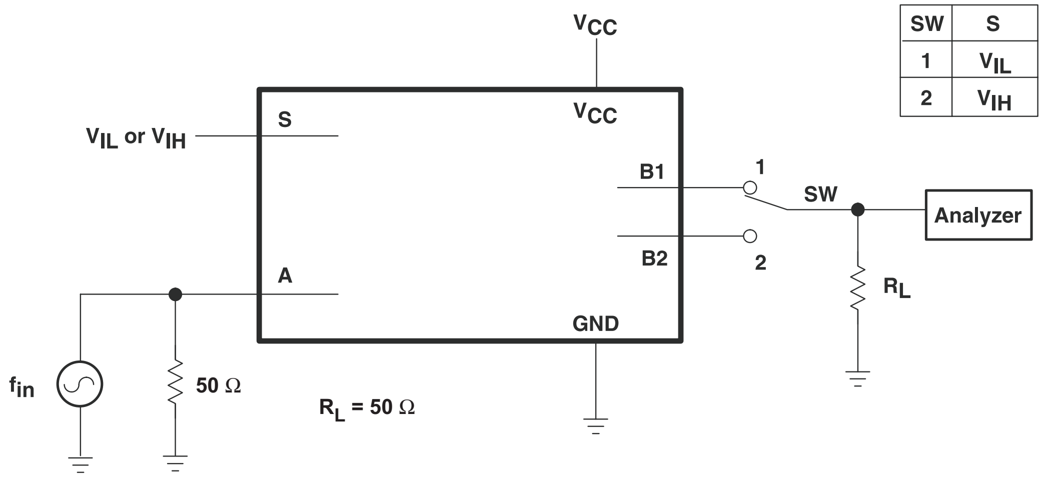


Figure 8. Feedthrough

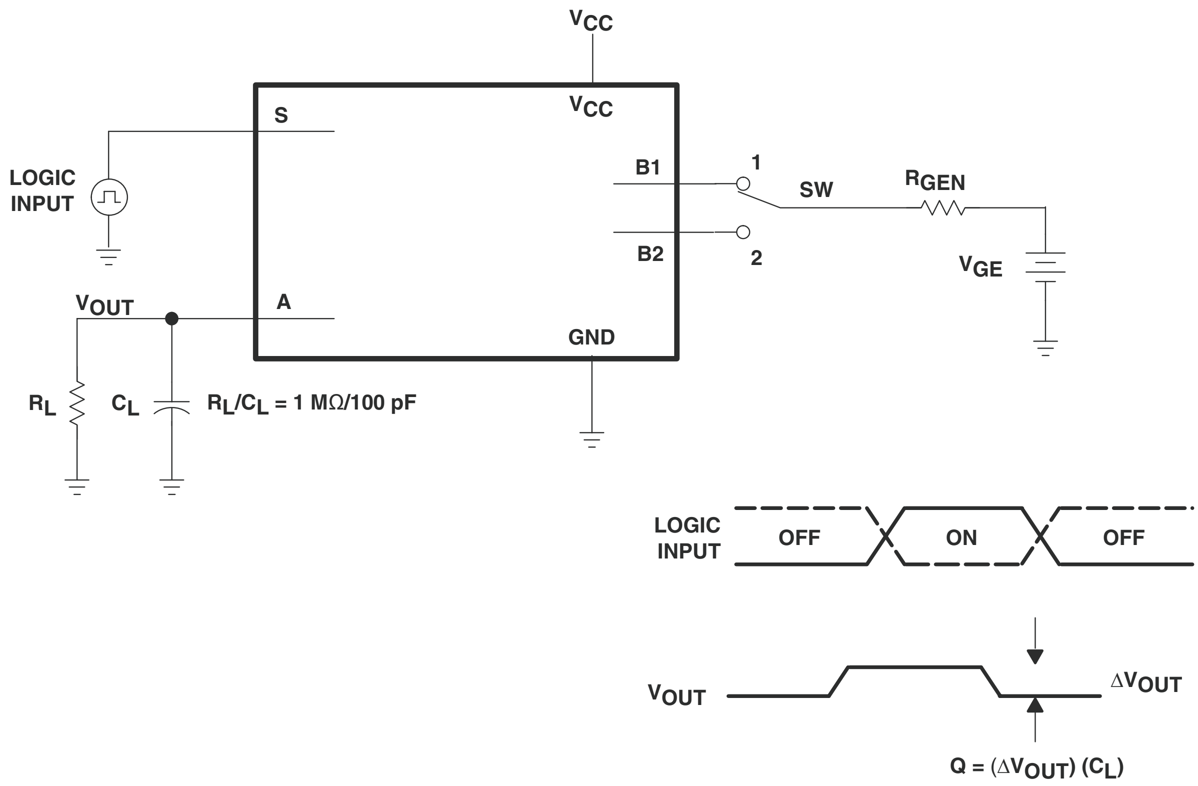
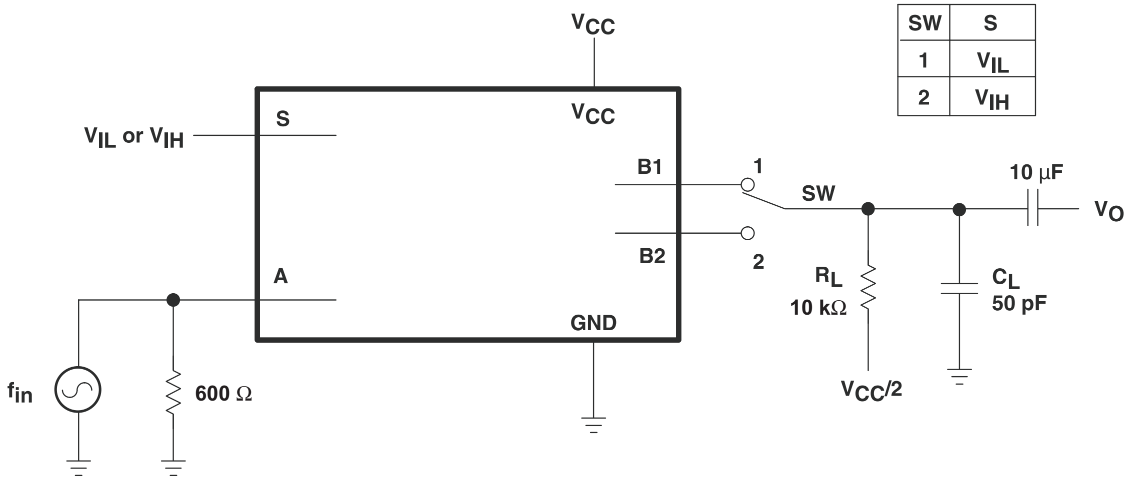


Figure 9. Charge-Injection Test

PARAMETER MEASUREMENT INFORMATION (continued)



V_{CC} = 1.65 V, V_I = 1.4 V_{P-P}
V_{CC} = 2.30 V, V_I = 2.0 V_{P-P}
V_{CC} = 3.00 V, V_I = 2.5 V_{P-P}
V_{CC} = 4.50 V, V_I = 4.0 V_{P-P}

Figure 10. Total Harmonic Distortion

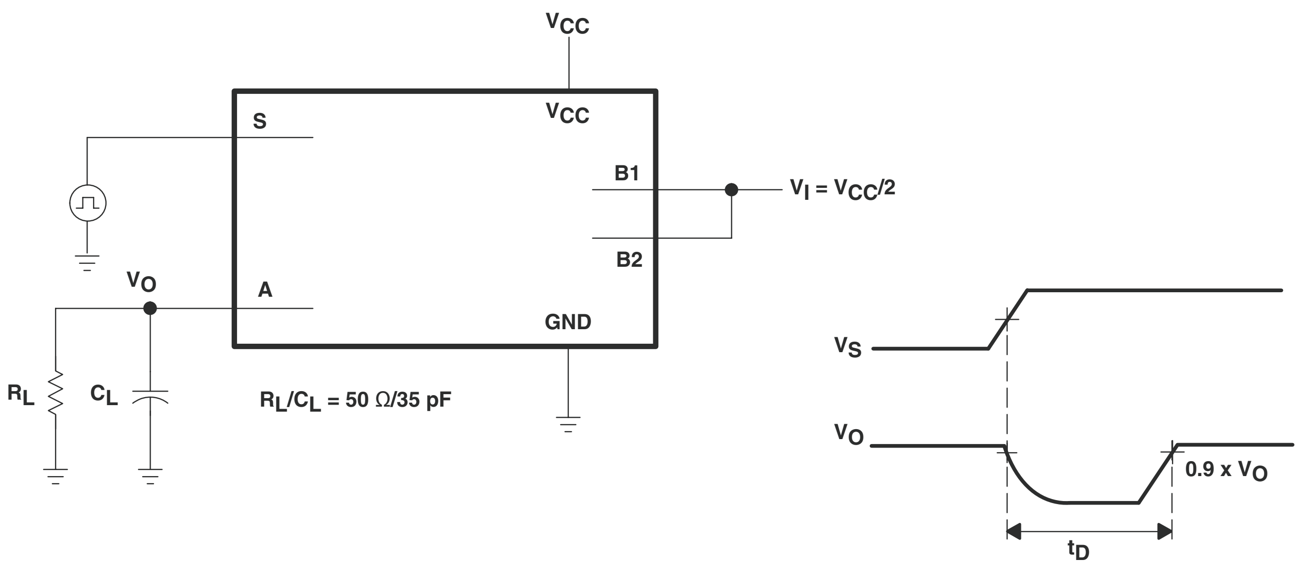


Figure 11. Break-Before-Make Internal Timing

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
74LVC1G3157DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G3157DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G3157DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G3157DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G3157DRLRG4	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G3157DRYRG4	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G3157DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G3157DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G3157DGVR	PREVIEW	SOT-23	DBV	6		TBD	Call TI	Call TI
SN74LVC1G3157DRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G3157DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G3157YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G3157 :

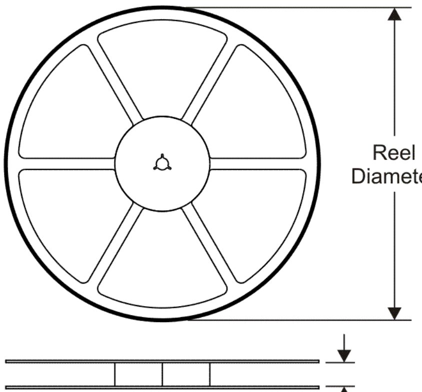
- Automotive: SN74LVC1G3157-Q1

NOTE: Qualified Version Definitions:

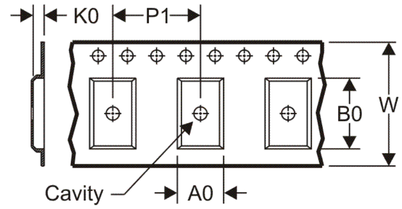
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

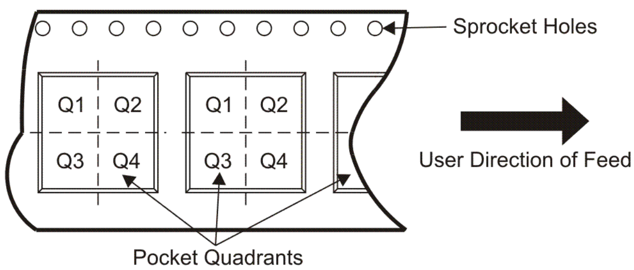


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

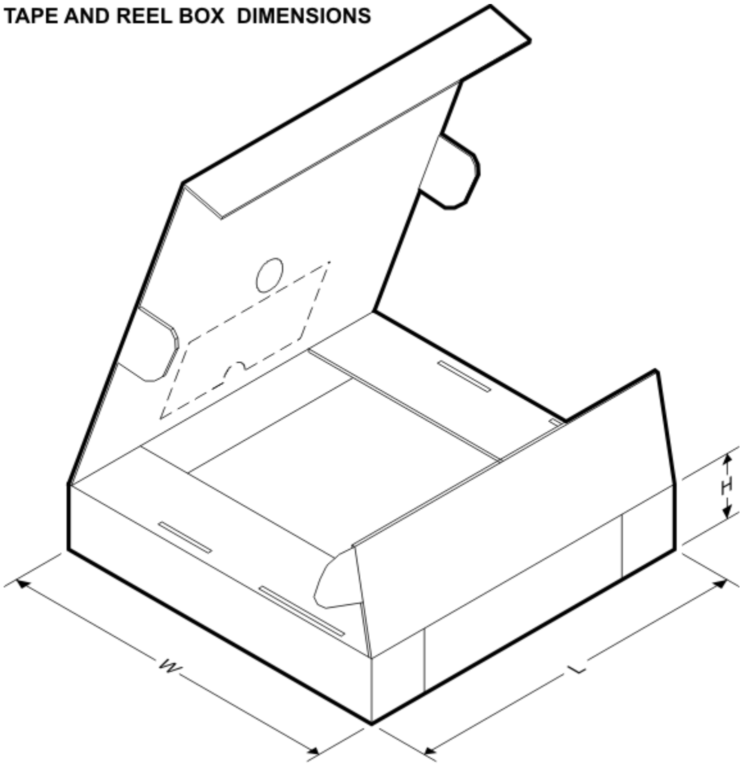
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	180.0	9.2	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G3157DCKR	SC70	DCK	6	3000	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3
SN74LVC1G3157DCKR	SC70	DCK	6	3000	180.0	8.4	2.24	2.34	1.22	4.0	8.0	Q3
SN74LVC1G3157DRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G3157DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1

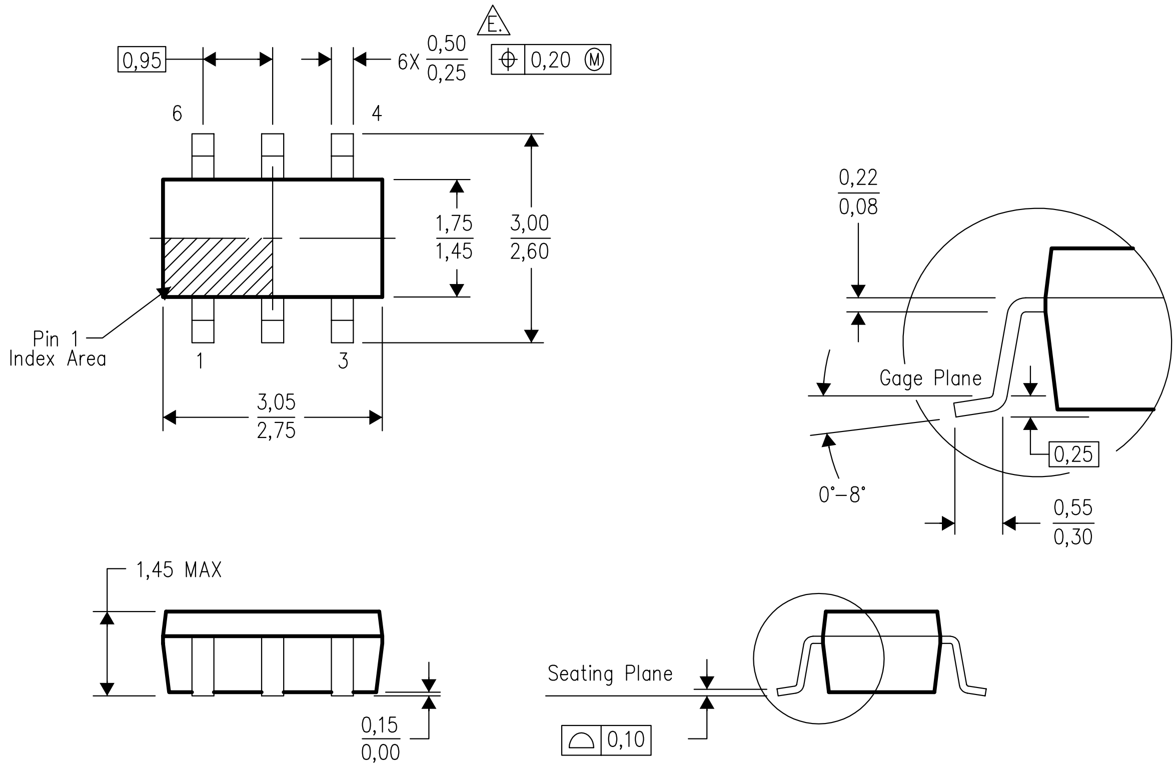
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	205.0	200.0	33.0
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1G3157DCKR	SC70	DCK	6	3000	205.0	200.0	33.0
SN74LVC1G3157DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74LVC1G3157DRLR	SOT	DRL	6	4000	202.0	201.0	28.0
SN74LVC1G3157DRYR	SON	DRY	6	5000	203.0	203.0	35.0
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	220.0	220.0	34.0

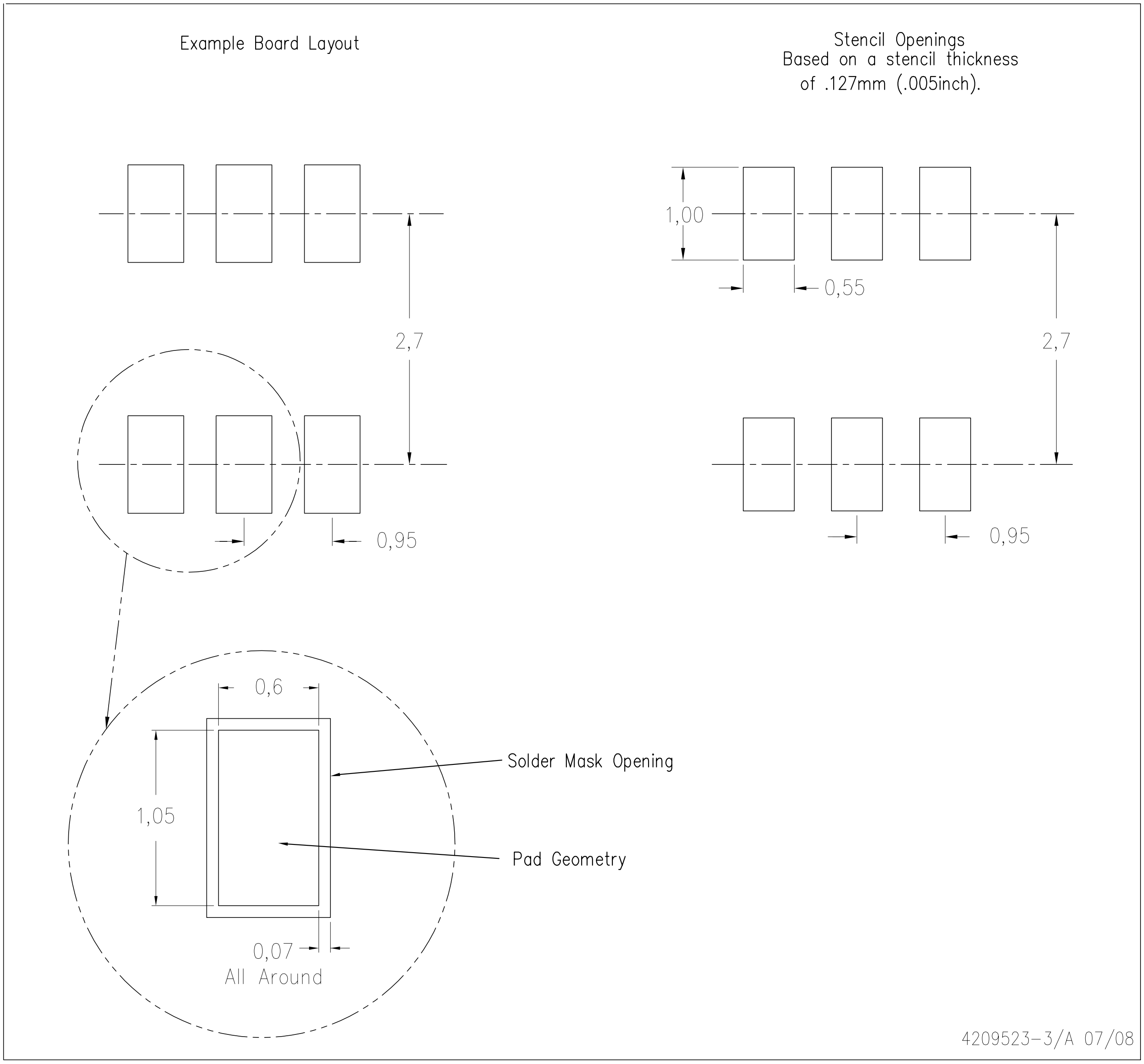
DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



4073253-5/K 03/2006

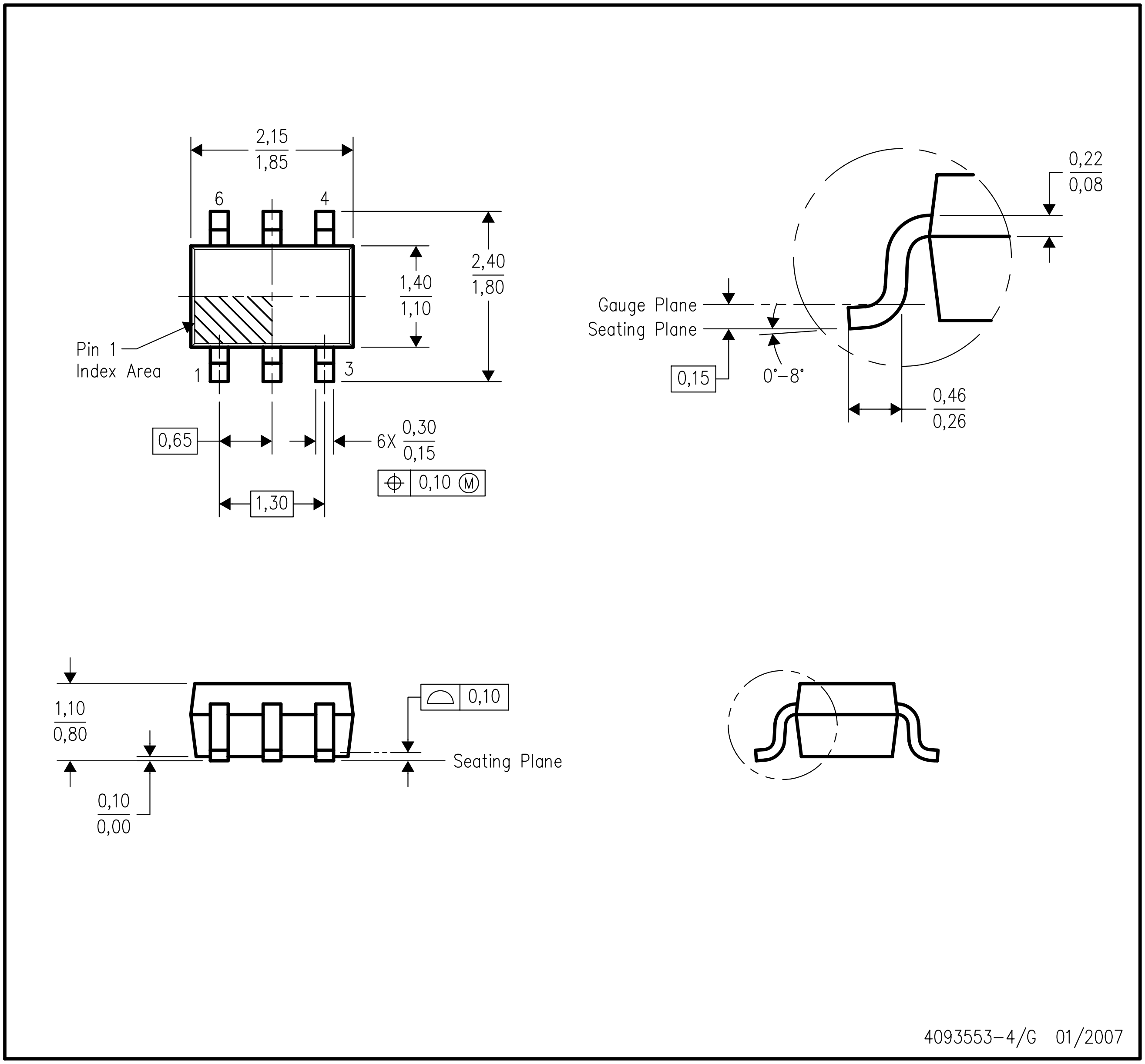
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)



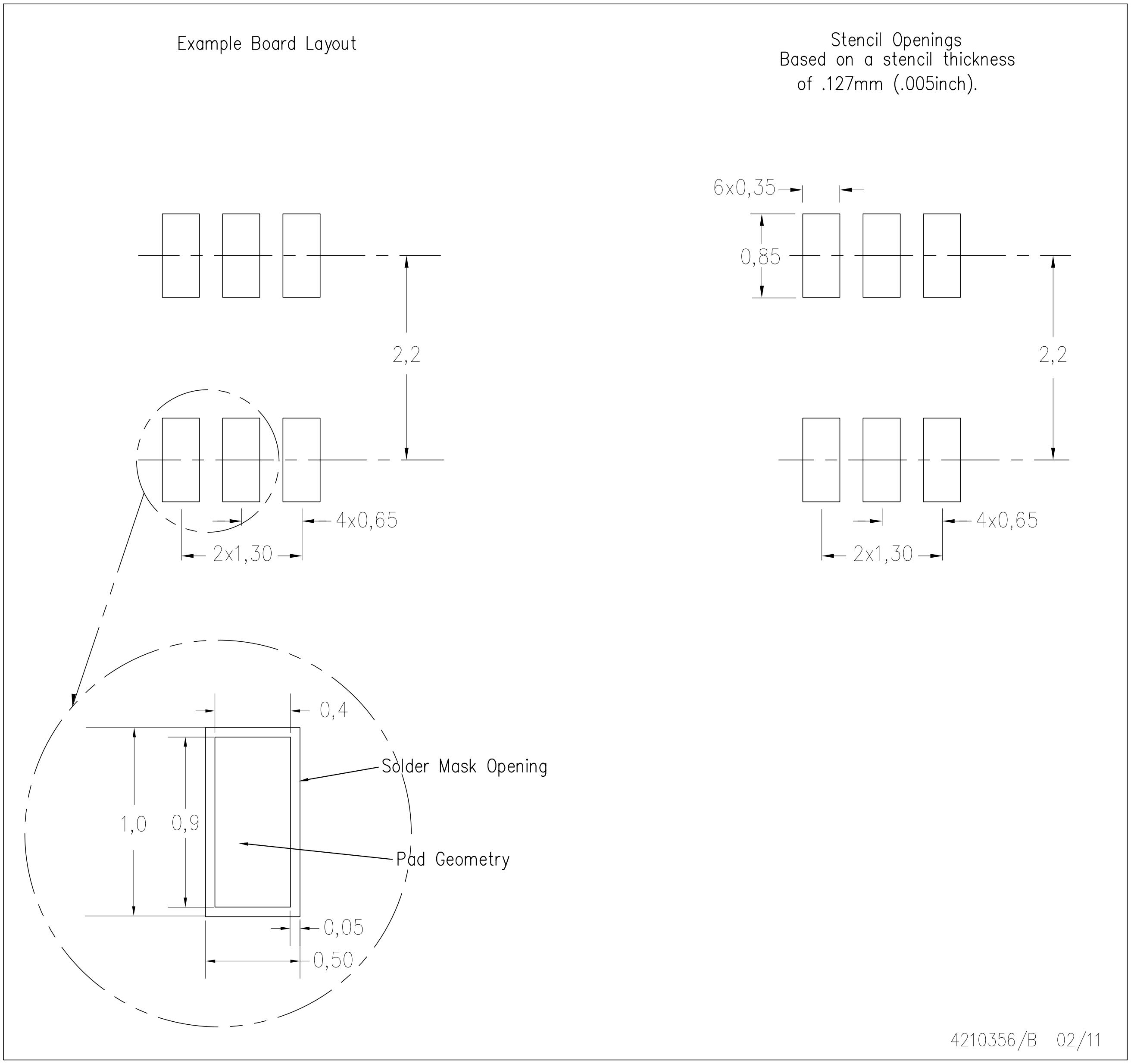
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE

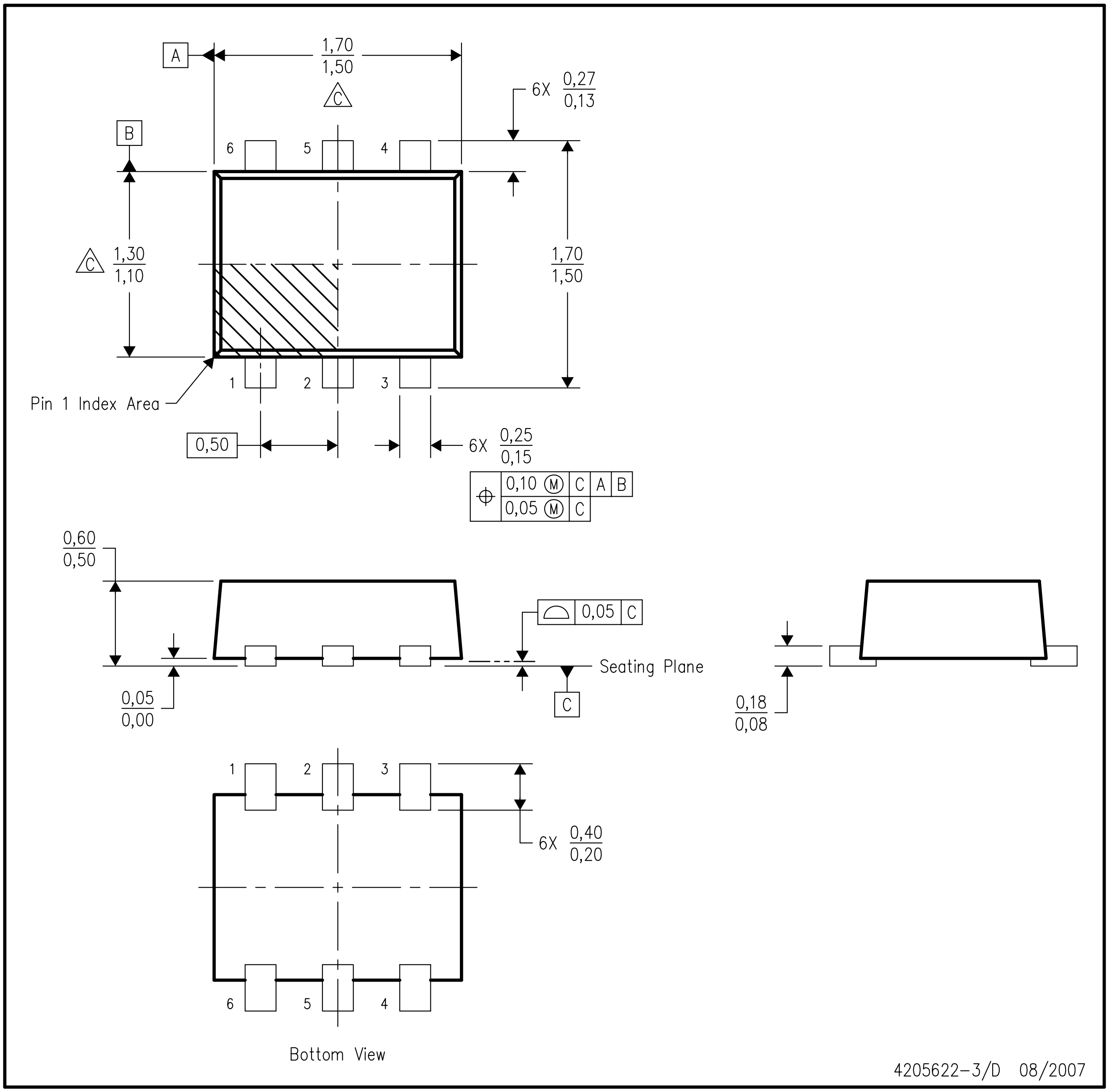


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.



NOTES:

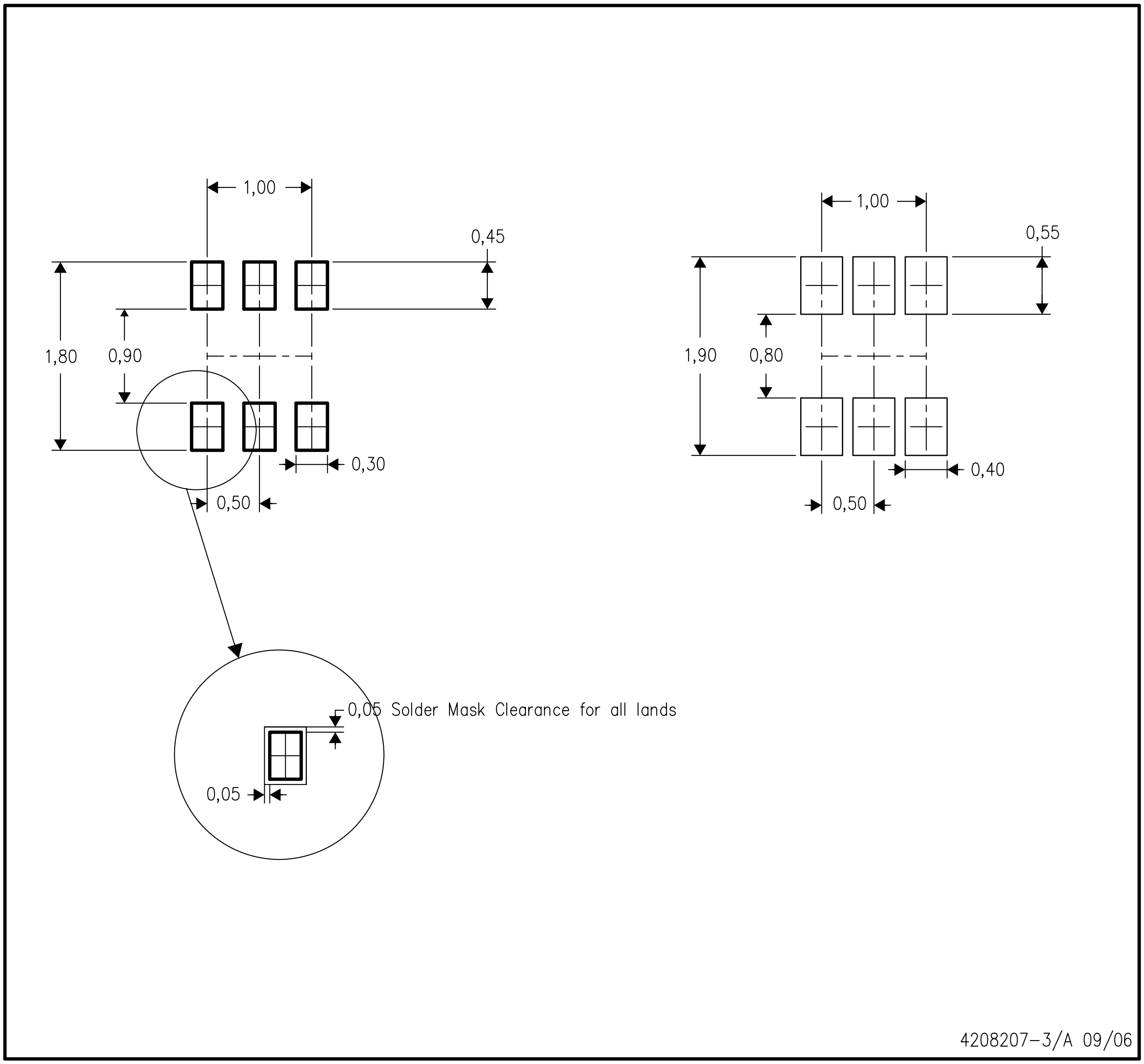
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.

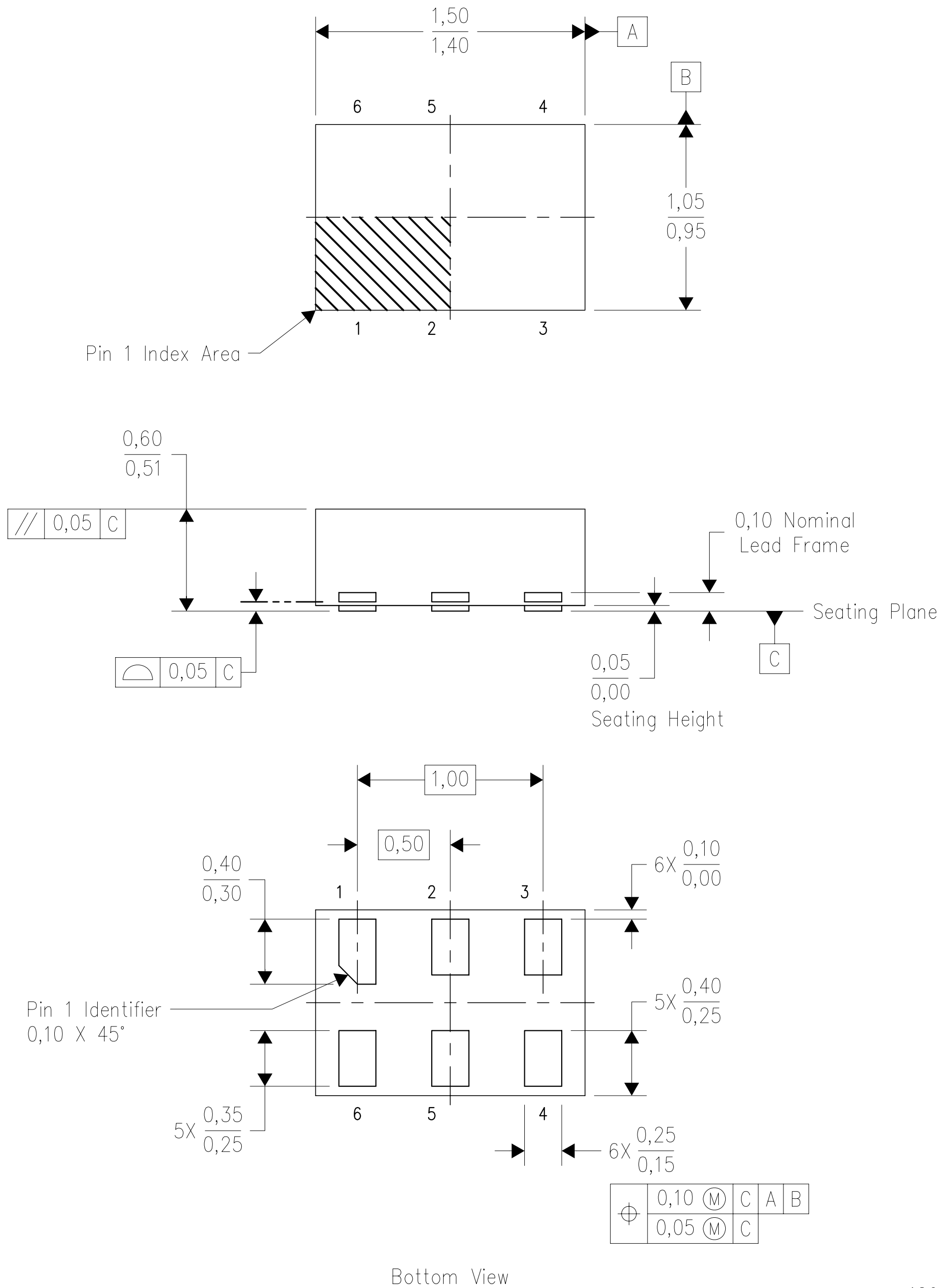
D. JEDEC package registration is pending.

DRL (R–PDSO–N6)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

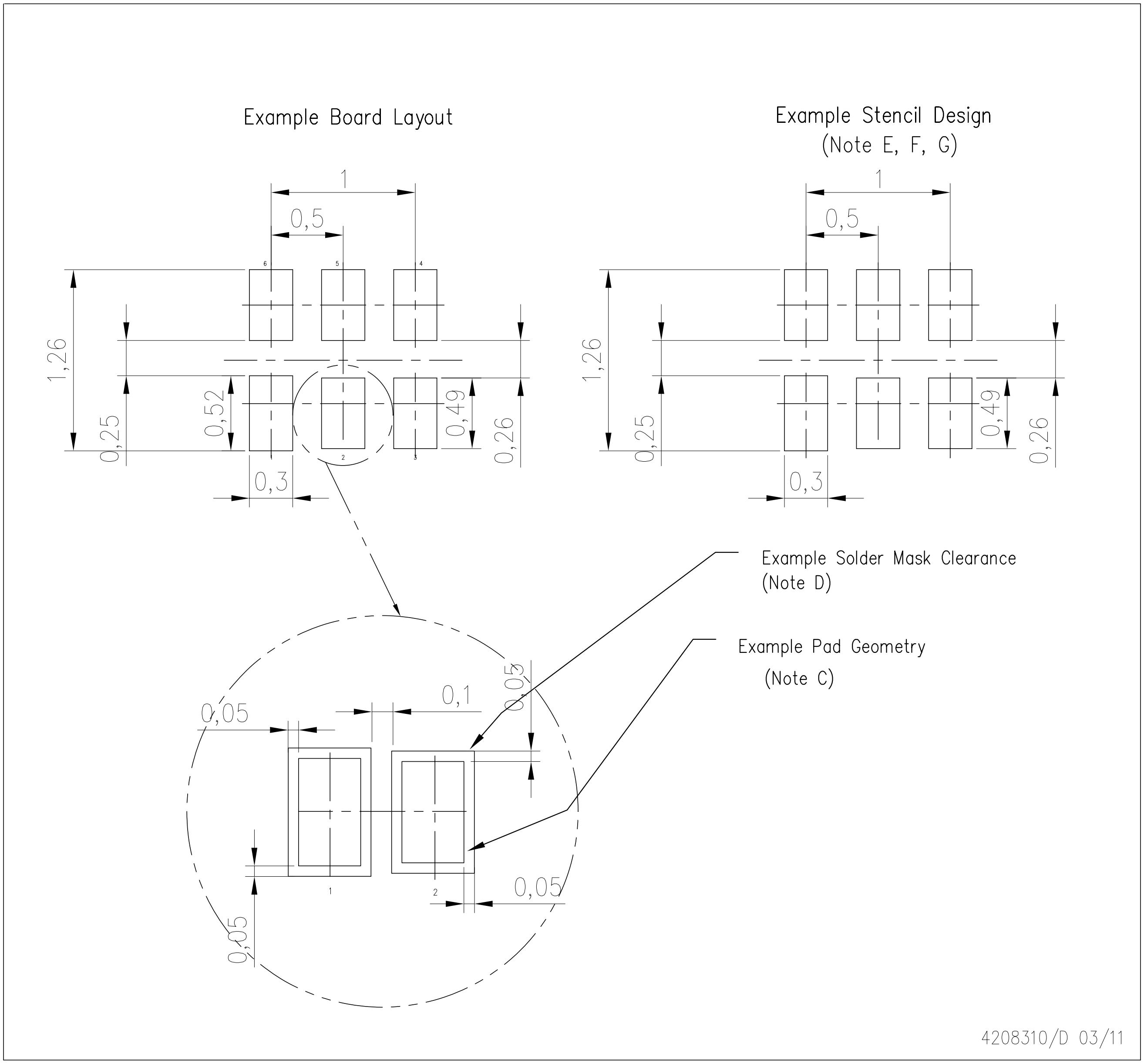
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4207181/D 12/10

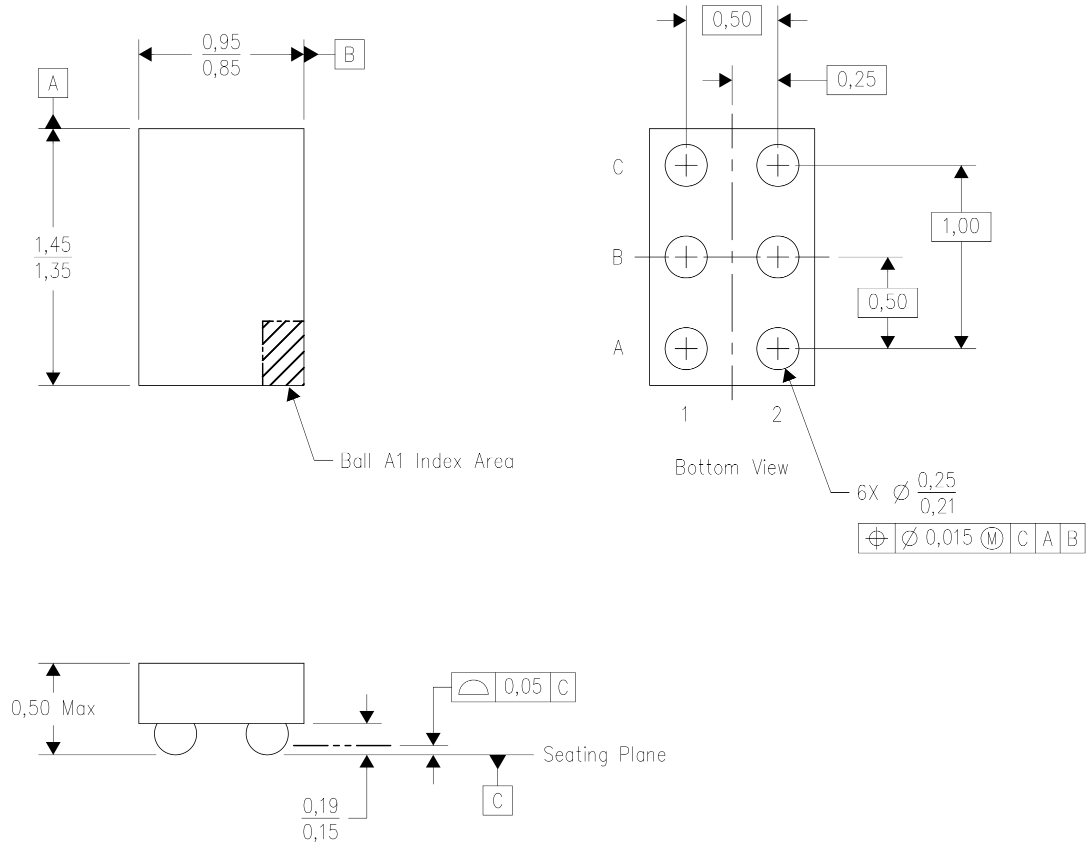
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. This package complies to JEDEC MO–287 variation UFAD.

DRY (S-PUSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

YZP (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY



4204741–3/G 07/2008

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. This package is lead–free. Refer to the 6 YEP package (drawing 4204725) for tin–lead (SnPb).

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